What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction;

a side wall formed on a side surface of said gate electrode so as to be covered behind a top part of said gate electrode as seen in plan view; and

an interlayer insulation film covering said gate electrode and being in contact with said side wall.

2. A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction;

a side wall formed on a side surface of said gate electrode so as to be covered behind a top part of said gate electrode as seen in plan view;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with said side wall.

3. A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction; and

a side wall formed on a side surface of said gate electrode so as to be covered behind a top part of said gate electrode as seen in plan view, said side wall being formed of a lamination of at least two insulation films having different etching properties.

4. The semiconductor device according to claim 1, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

5. The semiconductor device according to claim 2, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

6. The semiconductor device according to claim 3, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

7. The semiconductor device according to claim 4, wherein said gate electrode further comprises a visor part on said upper

part substantially constant and the greatest in the length along said gate length direction.

8. The semiconductor device according to claim 5, wherein said gate electrode further comprises a visor part on said upper part substantially constant and the greatest in the length along said gate length direction.

9. The semiconductor device according to claim 6, wherein said gate electrode further comprises a visor part on said upper part substantially constant and the greatest in the length along said gate length direction.

10. The semiconductor device according to claim 2, wherein said contact reaches a diffusion layer formed at a surface of said semiconductor substrate.

11. The semiconductor device according to claim 4, wherein said side walls are formed on a side surface of said upper part and on a side surface of said lower part out of different insulation films, respectively.

12. The semiconductor device according to claim 5, wherein said side walls are formed on a side surface of said upper part and on a side surface of said lower part out of different insulation films, respectively.

13. The semiconductor device according to claim 6, wherein said side walls are formed on a side surface of said upper part and on a side surface of said lower part out of different insulation films, respectively.

14. The semiconductor device according to claim 4, wherein a side surface of said upper part forms a tapered slope.

15. The semiconductor device according to claim 5, wherein

a side surface of said upper part forms a tapered slope.

16. The semiconductor device according to claim 6, wherein a side surface of said upper part forms a tapered slope.

17. A method of fabricating a semiconductor device comprising the steps of:

forming first and second insulation films on a semiconductor substrate in succession;

forming an opening of tapered shape, narrowing with depth, in said second insulation film;

forming an opening consistent with the bottom shape of said opening, in said first insulation film;

burying a conductive film into said openings formed in said first and second insulation films to form a gate electrode; and

etching said first and second insulation films with said conductive film as a mask to form a side wall on a side surface of said gate electrode so as to be covered behind a top part of said gate electrode as seen in plan view.

18. The method of fabricating a semiconductor device according to claim 17, further comprising the steps of, after forming said first and second insulation films:

forming a third insulation film on said second insulation film; and

forming an opening in said third insulation film onsistent with the top shape of said opening to be formed in said second insulation film, and

wherein forming an opening in said second insulation film is performed using said third insulation film as a mask.

19. The method of fabricating a semiconductor device according to claim 17, further comprising the steps of:

implanting ions into said surface of said semiconductor substrate with said conductive film as a mask to form a diffusion layer;

forming an interlayer insulation film covering said conductive film and diffusion layer; and

forming a contact hole reaching said conductive film and diffusion layer in said interlayer insulation film.

20. The method of fabricating a semiconductor device according to claim 18, further comprising the steps of:

implanting ions into said surface of said semiconductor substrate with said conductive film as a mask to form a diffusion layer;

forming an interlayer insulation film covering said conductive film and diffusion layer; and

forming a contact hole reaching said conductive film and diffusion layer in said interlayer insulation film.